

**We Claim:**

1           1. An integrated memory, comprising:  
2           a memory cell array, the memory cell array having word lines for selecting  
3 memory cells and bit lines for reading out or writing data signals;  
4           a read/write amplifier, the read/write amplifier being connected to the bit lines for  
5 assessing and amplifying data signals; and  
6           a voltage generator circuit for generating a voltage supply for application to the  
7 read/write amplifier, a potential difference being applied to the read/write amplifier using  
8 different supply potentials, the voltage generator circuit increasing the potential  
9 difference applied to the read/write amplifier for a limited period of time during an  
10 assessment and amplification operation of the read/write amplifier, wherein charge-  
11 dependent control is implemented in the voltage generator circuit to generate the  
12 increased potential difference using a defined quantity of charge.

1           2. The integrated memory as claimed in claim 1, wherein the voltage generator  
2 circuit increases a first supply potential at a first terminal of the read/write amplifier  
3 and/or lowers a second supply potential at a second terminal of the read/write amplifier  
4 during an assessment and amplification operation of the read/write amplifier.

1           3. The integrated memory as claimed in claim 1, wherein the voltage generator  
2 circuit has two supply paths for the read/write amplifier, the supply paths having a

3 different potential difference, the supply paths being driven alternatively to one another in  
4 time, the supply paths being connected to the read/write amplifier.

1 4. The integrated memory as claimed in claim 3, wherein at least two  
2 capacitances, the capacitances connected into the supply path which has a higher  
3 potential difference, the capacitances being connected to a respective supply potential, the  
4 capacitances being connected to the read/write amplifier in the limited period of time, and  
5 the capacitances being discharged and charged in this state.

1 5. The integrated memory as claimed in claim 4, wherein the  
2 that supply path which has a higher potential difference is driven by a pulse shaper, which  
3 generates a control pulse for the connecting up the capacitances at the beginning of an  
4 assessment and amplification operation of the read/write amplifier.